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Specialized Wirebond Process Configuration on Advanced Multi-Die Package

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

Wirebonding process is one important assembly process responsible for providing electrical connections between the silicon die and the external leads of a semiconductor package or device. The process also brings along some challenges as the device becomes more complex and critical. This paper is focused on the prevention of the broken wire on neck during wirebonding process of an advanced semiconductor package with multi-die configuration. Extensive wire loop characterization and optimization was done and a specialized wirebonding configuration solution was formulated. Ultimately, the solution prevented high loop and wire sagging that could touch or short-circuit the silicon die. For future works, the configuration could be applied on packages with comparable construction.

Keywords: Wirebond; assembly; semiconductor; multi-die configuration; stacked dice.

1. INTRODUCTION

Semiconductor package miniaturization and continuous technology trends have provided manufacturability challenges especially on advanced packages. One important assembly process usually affected is the wirebonding process. Assembly manufacturing obstacles are

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inevitable during package development of an advanced semiconductor package with multi-die configuration as shown in Fig. 1. One great challenge is the difficulty on wire looping during wirebonding process at the bottom die. A critical aspect to consider is the avoidance of the wire-to-die shorting between the wires and bottom die especially during the die attach process of the succeeding top die. With this scenario, wire looping characterization and optimization is critically needed to satisfy the requirements in wirebonding process.

2. LITERATURE REVIEW AND PROBLEM IDENTIFICATION

Wirebonding is the process of providing electrical connections using very fine bondwires (or simply wires) through combination of heat, pressure and thermosonic energy between the silicon die and the external input/output (I/O) leads of the semiconductor device. The wire used is usually made either of gold or aluminum, although copper wires are starting to gain attention in the semiconductor assembly manufacturing industry [1-4]. One common wirebond process is the ball bonding and is one of the most challenging processes in assembly manufacturing. Fig. 2 shares the overview of the ball bonding wirebond process.

An overview of the assembly process flow applicable for the device in focus is shared in Fig 3. It is worth noting that process flow varies with the product and the technology [5-9]. As mentioned earlier, with new and continuous technology trends and breakthroughs, challenges in assembly manufacturing are inevitable [10-12].

Fig. 1. Multi-die package design cross-section

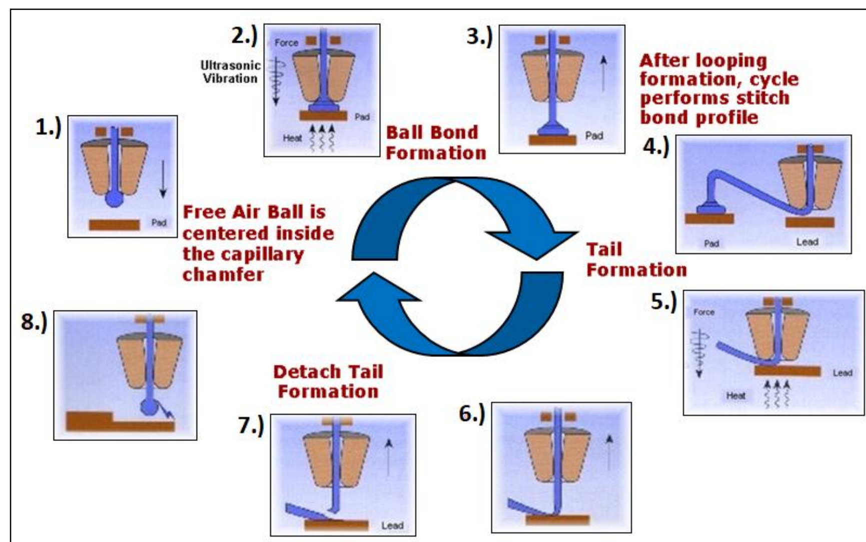

Fig. 2. Ball bonding wirebond process mechanism

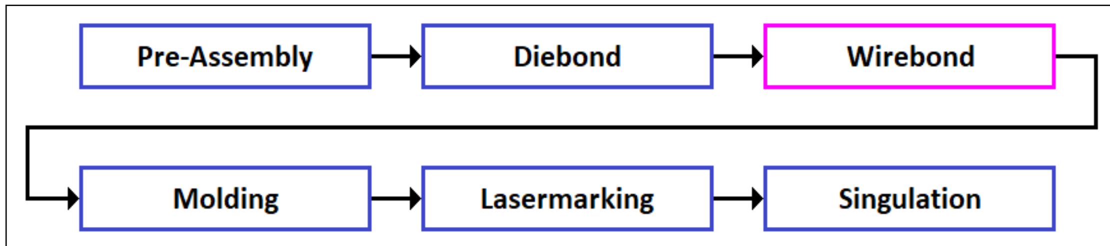

Fig. 3. Assembly process flow

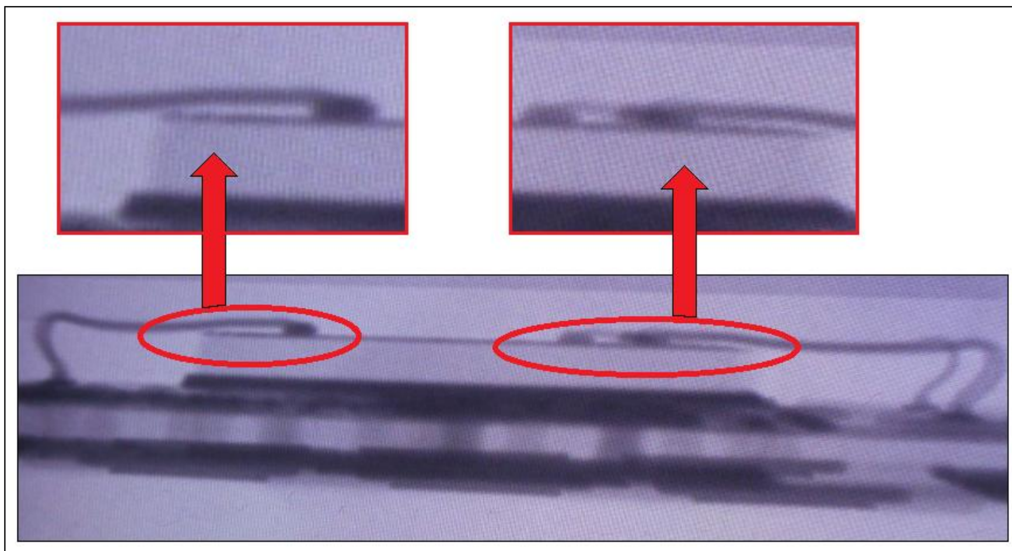

Fig. 4. Tight loop on wirebonding process

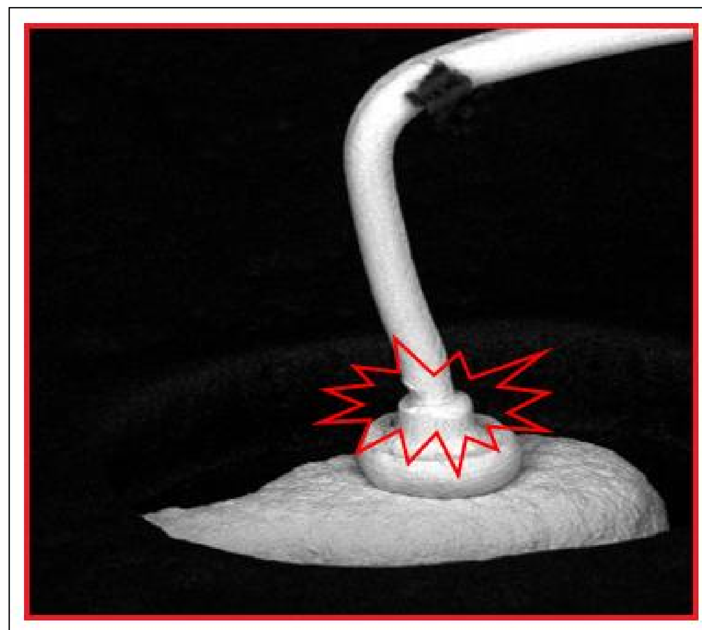

Fig. 5. Broken wire on neck defect

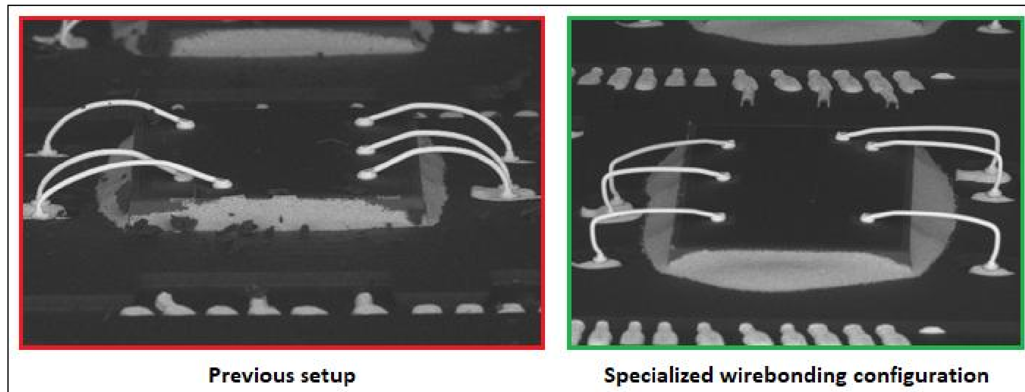

Fig. 6. Improved loop formation with no observed broken wire on neck defect

During wirebonding process at bottom die, a criticality in the loop was seen and anticipated due to the succeeding die attach process of the top die. The condition for the loop was for the top of wire not to short-circuit or touch with either of the two dies, assembled on a critical stacked dice configuration. Also, it is difficult to determine visually due to very tight clearance with few micron (μm) difference as emphasized in Fig. 4.

Optimization of wire looping is very challenging because of the kink or sharp bend. In this case and with very tight clearances, the issue resulted to broken wire on neck or nicking as seen in Fig. 5.

3. PROCESS DEVELOPMENT SOLUTION AND DISCUSSION OF RESULTS

An improved and specialized solution in wirebonding process is extensively done with wire looping optimization. The solution employed wire looping characterization and optimization on the wirebonding process at bottom die as shown in Fig. 6, preventing high loop and wire sagging that could touch the succeeding top die. Furthermore, no broken wire on neck occurrence was observed during the wirebonding process.

The optimized loop parameter eventually served as the good loop formation, which also passed the destructive wire-pull test.

4. CONCLUSION

With the comprehensive wirebond process characterization and optimization, wire loop solution was successfully achieved for the advanced semiconductor package with very tight clearances on its multi-die configuration. The improved solution prevented high loop and wire sagging that could short-circuit or touch the silicon die. Moreover, no broken wire on neck or nicking was observed during the process. This specialized wirebond configuration is considered a key milestone which could be used for future works on any other semiconductor devices with similar construction.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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